Multiple Input Queueing in Packet Switches

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***Abstract*— In this letter we mainly discuss the derivation of the Multiple Input Queueing (MIQ) and Virtual Output Queueing (VOQ) techniques applied in packet switching.**

***Index Terms*— Packet switching, multiple input queueing, virtual output queueing.**

IN IEEE Communications Letters, vol. 1, no. 2, pp. 56-57, March 1997, a letter on "Bifurcated Queueing for Throughput Enhancement in Input-Queued Switches" appeared, authored by G. Thomas. Herewith and with reference to the above publication, we reflect on the origin of the Multiple Input Queueing (MIQ) technique and on the concept of Virtual Output Queueing (VOQ), applied to input-queued packet switching. The concept of Multiple Input Queueing (MIQ), was first proposed and analyzed by the authors in our 1996 paper [2] which was prior to Thomas' publication and other references (i.e., [4]). The MIQ technique was presented as an extension and continuation of our work on the "Odd-Even" switch [1], while in [2] a generalization of the MIQ technique, namely VOQ, was presented. Under MIQ, each switch's input-port holds a number of discrete queues for storing incoming traffic, as opposed to a switch with a single FIFO input queue per port (which exhibits the well-known Head-of-Line blocking problem). In fact, we introduced two schemes with respect to implementing MIQ. The corresponding analytical and simulation results were included.

We proved that, if each input port in an input-queued switch can hold m FIFO queues for buffering incoming packets, for instance, according to their output port destination (thus each of the m input queues is associated with a distinct subset of output ports), then the switch's maximum attainable throughput is, under certain conditions, $\gamma_{max} = 1 + m - \sqrt{1+m^2}$. For $m = N$ (where N is the switch size), we called this special case of MIQ, *Virtual Output Queueing* (VOQ) [2], as, essentially, a Virtual Output Queue holds and switches packets that are all destined to the same output port, without having to incur the associated cost that accompanies pure output-queued switches (i.e., using speedup). Additional packet-switching architectures, analytical and simulation results can be found in [3].

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Manuscript received December 2, 2007. The associate editor coordinating the review of this letter and approving it for publication was C. Georghiades.

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Digital Object Identifier 10.1109/LCOMM.2008.072027.